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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,554	08/06/2001	Masahito Matsuo	027260-482	7038

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EXAMINER	
GERSTL, SHANE F	
ART UNIT	**PAPER NUMBER**
2183	5

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/921,554	MATSUO, MASAHITO
	Examiner	Art Unit
	Shane F Gerstl	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/6/01, 9/14/01, and 3/31/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 have been examined.

Papers Received

2. Receipt is acknowledged of priority, information disclosure statement, and power of attorney papers submitted, where the papers have been placed of record in the file.

3. Tin regard to the communication including power of attorney papers submitted on 31 March 2003, the examiner requests confirmation that this communication validly pertains to this application, number 09/921,554. The application number on the communication matches this case, however, the inventorship (Talley et al.), examiner (Cabeca, John W.), group (2173), filing date (August 2, 2001), and title (Graphical List Grouping Widget and Methods of Use Thereof) are all inconsistent with the immediate application.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Repeat Processing by Inhibiting Remaining Instructions After a Break in a Repeat Block by Converting them to No-operation Instructions.

Claim Objections

6. Claim 5 is objected to because of the following informalities: lines 6-7 shows the phrase "of last instruction," which in proper grammatical form, and to avoid antecedent basis, should be rewritten as "of a last instruction." Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 1 recites the limitation "the execution of the remaining instructions " in lines 10-11. There is insufficient antecedent basis for this limitation in the claim. First, there has been no previous execution defined in the claim and so it is unclear whether "the execution" is referring to a previous state of execution or not. The examiner is taking the phrase to simply mean "execution" so that it is understood that execution in general is inhibited. Also, there has been no occurrence of remaining instructions of the repeat block defined so it is unclear as to what the remaining instructions are. The examiner is interpreting the phrase to mean "remaining instructions" so it is understood that any remaining instructions that may exist are inhibited.

10. Claim 3 recites the limitation "the next instruction" in line 21. There is insufficient antecedent basis for this limitation in the claim. The examiner is taking the claim to

mean "a next instruction" since no previous "netx instruction" had yet been defined in the claim tree.

11. Claim 4 recites the limitation "the next instruction" in line 27. There is insufficient antecedent basis for this limitation in the claim.

12. Claim 6 recites the limitation and "the last instruction" in line 12. There is insufficient antecedent basis for this limitation in the claim. The examiner is taking "the last instruction" to mean "a last instruction since the definition of this last instruction is given after the limitation so it is known what particular instruction is meant by last.

13. Claim 8 recites the limitation "the number of repetitions" in line 21. There is insufficient antecedent basis for this limitation in the claim. The examiner is taking the claim to mean "a number of repetitions."

14. Claim 8 recites the limitation "the last instruction" in line 24. There is insufficient antecedent basis for this limitation in the claim. The examiner is taking "the last instruction" to mean "a last instruction since the definition of this last instruction is given after the limitation so it is known what particular instruction is meant by last.

15. Claim 9 recites the limitation "the number of instructions" in line 6. There is insufficient antecedent basis for this limitation in the claim. The examiner is taking the claim to mean "a number of repetitions."

16. Claim 10 recites the limitation "the count number " in line 12. There is insufficient antecedent basis for this limitation in the claim. The examiner is taking the claim to mean "a count number."

17. Claim 11 recites the limitation "the number of repetitions" in line 16. There is insufficient antecedent basis for this limitation in the claim. The examiner is taking the claim to mean "a number of repetitions.

18. Claim 11 recites the limitation "the count number" in line 20. There is insufficient antecedent basis for this limitation in the claim. The examiner is taking the claim to mean "a count number."

19. Claim 11 recites the limitation "the last repeat processing" in line 22. There is insufficient antecedent basis for this limitation in the claim. The examiner is taking the claim to mean "a last repeat processing."

20. Claim 3 and 4 are very unclear as to how the instruction processing sequence switches to a next instruction of the repeat block when the parent claim has specifically stated that remaining instructions are inhibited from being executed. The examiner taking claim 4 to mean that the execute stage processes remaining instructions in the pipeline after a break but converts them to NOPs before switching to them effectively inhibiting the original instruction from being executed as taught in the specification, but this NOP is not the next instruction of the repeat block, it is a substitute instruction. The examiner is taking claim 3 to mean that the next instruction after the break in the repeat block is fetched.

21. Claims 5 and 6 are very unclear as to how one would jump to a next instruction in a block of instructions when the current instruction is a last instruction that is executed last in the block. In such a case there would be no next instruction in the block. The examiner is taking the claim to mean that upon reaching the end of a repeat block, the

next instruction to be repeated is jumped to. Also, it is unclear what "jump processing" is. The examiner is taking this term to mean all steps that take place from executing a jump to fetching the target for processing.

Claim Rejections - 35 USC § 102

22. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

23. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Sato (6,345,357).

24. In regard to claim 1, Sato discloses a data processor which executes a program including a repeat block composed of plural instructions and processed repeatedly (column 15, line 62 – column 16, line 47 show an embodiment using both step-repeat and block-repeat processing with details discussed prior in the document), said data processor comprising:

a. detecting means implemented by hardware, for detecting a break of repeat processing in said repeat block independently of an operation specified by an instruction being executed; Column 12, line 63 – column 13, line 18 show that a repeat end flag is detected and indicates that the number of repeats is completed and thus the repeat block is broken. This is shown to have no

dependencies on the actual operation being executed anywhere in the disclosure.

b. and instruction execution inhibit means responsive to the detection of said break of said repeat processing by said detecting means to inhibit the execution of the remaining instructions in said repeat block. As shown in column 12, line 63 – column 13, line 18, after detecting this repeat end flag, remaining instructions in the repeat block are negated or set to NOP and effectively inhibited. This is further shown in column 13, line 65 - column 14, line 18 with figures 11-12 that illustrate that remaining instructions N+8 to N+11 in a repeat block are converted to NOPs and thus inhibited.

25. In regard to claim 2, Sato discloses the data processor according to claim 1, wherein said instruction execution inhibit means is means implemented by hardware for converting said remaining instructions in said repeat block to no operation instructions upon detection of said break of said repeat processing by said detecting means as shown above.

26. In regard to claim 3, Sato discloses the data processor according to claim 1, wherein said instruction execution inhibit means is instruction processing sequence switching means for switching said instruction processing sequence to the next instruction of said repeat block at an instruction fetch stage upon detection of said break of said repeat processing by said detecting means. Column 13, line 65 - column 14, line 18 shows that the next instruction after the break is fetched.

27. In regard to claim 4, Sato discloses the data processor according to claim 1, wherein said instruction execution inhibit means is instruction processing sequence switching means for switching said instruction processing sequence to the next instruction of said repeat block at an instruction execution stage upon detection of said break of said repeat processing by said detecting means. As shown above, remaining instructions of a repeat block are converted to NOPs and are executed as such and thus the execute stage points to the next instruction (which has been converted to a NOP) in the repeat block after the break is detected.

28. In regard to claim 5, Sato discloses the data processor according to claim 4, wherein said instruction processing sequence switching means is means for performing jump processing to the next instruction of said repeat block during execution of last instruction that is executed last in said repeat processing of said repeat block. Column 7, line 64 – column 8, line 9 show that the last instruction in a repeat block is detected and the starting address of the block (SRPT_S) is transferred over the JA (jump address) bus. Column 8, lines 20-26 show that the first address of the repeat block is jumped to in the execution stage. This is also illustrated in column 10, lines 50-61.

29. In regard to claim 6, Sato discloses the data processor according to claim 4, wherein said instruction processing sequence switching means is means for performing jump processing to the next instruction of said repeat block after execution of the last instruction that is executed last in said repeat processing of said repeat block. Since jump processing is taken to include fetching the target of the jump for processing, this

fetching takes place after the execution of the actual jump, which stimulates the fetching of the target as shown by Sato.

30. In regard to claim 7, Sato discloses the data processor according to claim 1, wherein said detecting means is means for deciding whether said repeat processing breaks, based on an address of an instruction that is executed during said repeat processing of said repeat block. Column 10, lines 50-61 show that if the last instruction is detected and the counter is still above 1, control is changed over (to the beginning of the repeated section), and thus a break is not set forth, effectively showing a break would be set forth in the case where the counter was at 0. This is indeed shown to be the case in column 12, line 63 – column 13, line 18 that the counter at zero signifies a break in repeat processing.

31. In regard to claim 8, Sato discloses the data processor according to claim 7, wherein said detecting means has count means for counting the number of repetitions of processing of said repeat block, and comparison means for comparing the address of the instruction to be currently processed in said repeat block with the address of the last instruction to be executed last in said repeat processing of said repeat block, and wherein upon being informed from said comparison means of the coincidence of address between said instruction to be currently processed and said last instruction when the count number of said count means has reached a predetermined value, said detecting means decides that said repeat processing breaks as shown above.

32. In regard to claim 9, Sato discloses the data processor according to claim 1, wherein said detecting means is means for deciding whether said repeat processing

breaks, based on the number of instructions to be executed during repeat processing of said repeat block. Column 7, lines 55-63 show that the SRPT_C register holds the count of executions of instructions for repeating. Column 8, lines 10-14 show that this number is decremented after each instruction execution and column 12, line 63 – column 13, line 18 show that there is a break when the counter is 0.

33. In regard to claim 10, Sato discloses the data processor according to claim 9, wherein said detecting means has count means for counting the number of instructions executed during said repeat processing of said repeat block, and decides that said repeat processing breaks when the count number of said count means reaches a predetermined value. As shown above the counter SRPT_C down counts the number of instructions to be executed and breaks at predetermined value 0.

34. In regard to claim 11, Sato discloses the data processor according to claim 9, wherein said detecting means has first count means for counting the number of repetitions of processing of said repeat block and second count means for counting the number of instructions executed during each repeat processing of said repeat block, and said detecting means decides that said repeat processing breaks when the count number of said first count means reaches a first predetermined value and the count number of said second count means reaches a second predetermined value in the last repeat processing of said repeat block. As shown above, the counter down counts the number of instructions to be executed and breaks at predetermined value 0. As shown in column 15, line 62 – column 16, line 47, this counter also tracks repeat block iterations in the same manner and looks for predetermined value 0.

Conclusion

35. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the art with respect to repeat processing in general.

US Pat No 5,752,015 to Henry teaches inhibiting instructions in a repeat block by inserting NOPs.

US Pat No 6,079,008 to Clery, III discloses replacing instructions in loops with NOP instructions so as to inhibit them.

US Pat No 6,085,315 to Fleck shows replacing instructions in loops with NOP instructions to inhibit them.

US Pat No 6,263,489 to Olsen illustrates skipping instructions of a loop by converting them to NOPs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7305. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
May 28, 2004

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